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Description

GATE CONTROLLED FLOATING WELL VERTICAL MOSFET

BACKGROUND OF INVENTION

[0001] The present invention related generally to MOSFET devices, and specifically to a novel floating well vertical MOSFET device implementing a gate control means for use in Dynamic Random Access Memory (DRAM) cell applications.

[0002] The key challenge in scaling of MOSFET is to improve the drive current and to keep sufficiently low off-state leakage current. As the gate oxide and channel length are scaled down, the operating voltage has also been scaled down continuously. The threshold voltage can not be scaled down as aggressively as the operating voltage because of the subthreshold leakage. Therefore, the gate over-drive is reduced while keeping low leakage in off-state. One possible solution is the dynamic threshold voltage MOSFET (DT-MOSFET) which connects the gate to a

well. In the DT-MOSFET, high drive current and low off current can be obtained because of low threshold voltage in on-state and high threshold voltage in off-state. Unfortunately, the leakage current of the forward biased pn-junction at the source fatally increases at supply voltage higher than 0.7V. Therefore, the supply voltage must be reduced to be below 0.7V. In DRAM application, off-state leakage current, which limit the retention time, is very critical. Negative word line voltage has been proposed to reduce the off-state subthreshold leakage while keeping enough gate over-drive especially at write back conditions when the source of the transistor is near bit line high voltage level. With the negative word line low approach, another voltage source is needed and the device is more prone to gate induced drain leakage (GIDL) current.

[0003] It would thus be highly desirable to provide a floating well vertical MOSFET device implementing a gate control means to enable greater gate over-drive and drive currents.

Summary of Invention

[0004] According to one aspect of the invention, there is provided a novel transistor structure for a DRAM cell. The DRAM cell comprises two deep trenches, one trench com-

prising a storage cell for storing the data and the second trench comprising a control cell for controlling the p-well voltage, which, in effect, places part of the p-well in a floating condition thus decreasing the threshold voltage as compared to when the transistor is in an off-state. This enables the transistor to exhibit increased gate over-drive and drive current. In accordance with this aspect of the invention, the storage cell comprises a floating well vertical MOSFET device.

[0005] In a first embodiment, the storage cell includes a vertical pass transistor having a gate, and source and drain regions formed in a p- well, the drain region formed by a diffusion in said p- well outside the deep trench capacitor adjacent a first buried strap to conduct voltage to the trench capacitor. The control cell for controlling the threshold voltage of the vertical pass transistor, includes a second buried strap and diffusion region formed in the p-well region. According to the first embodiment, the second buried strap and diffusion region formed in the p-well region of the control cell is at a lower trench depth than the first buried strap and drain diffusion region formed in the p- well region of the storage cell. In this embodiment, the threshold voltage of the vertical pass

transistor is controlled in accordance with a depletion region formed by application of the WL voltage, via a control cell gate, at the second buried strap region and diffusion region that extends sufficiently into the p-well to pinch off the p- well region to disconnect the p-well region into two regions, a first conductive and second floating p-well region, wherein the floating p-well region enables a lower threshold voltage for turning on the vertical pass transistor during WL active state. When the WL voltage indicates inactive state, the depletion region formed at the second buried strap and diffusion region does not pinch off the p-well. Thus, no floating p-well region is created resulting in no threshold voltage modification.

[0006] According to a second embodiment, a vertical transistor device having two trenches is shown including respective two first buried straps functioning as a drain or source diffusion region for the device and two second buried straps functioning as control diffusions are formed in the p- well region. In the transistor device, the two first buried straps are at an equal trench depth and the two second buried strap and control diffusions are at an equal trench depth below the corresponding first buried straps formed in the p- well. In this embodiment, the threshold

voltage of the vertical transistor device is controlled in accordance with depletion regions formed by application of a voltage at the device gates, at both first and second buried strap region and diffusion regions, that extend sufficiently into the p-well and merge to effectively pinch off the p- well region to disconnect the p-well region into two regions, a first conductive and second floating p-well region, wherein the floating p-well region enables a lower threshold voltage for turning on the vertical pass transistor.

[0007] According to a further aspect of the invention, there is provided a method for manufacturing the novel DRAM cell of the invention. The novel DRAM structure of the present invention is fabricated with 110 nm, or less, vertical MOSFET DRAM fabrication technology.

Brief Description of Drawings

[0008] Further features, aspects and advantages of the structures and methods of the present invention will become better understood with regard to the following description, appended claims, and accompanying drawings with like elements represented by like reference numerals in the various figures, in which:

[0009] Figure 1 depicts a cross-sectional view of the DRAM cell

10 having a storage cell 20 and a control cell 30 separated by a p-well region 45 according to the present invention;

[0010] Figures 2(a) and 2(b) illustrate the operation of the novel DRAM control cell 30 for controlling the p-well voltage according to a first embodiment of the invention; and,

[0011] Figures 3(a) and 3(b) illustrate the operation of a novel vertical transistor device of two trenches for controlling the p-well voltage according to a second embodiment of the invention;

[0012] Figures 4(a)-4(o) depict the method for manufacturing the DRAM cell according to the first embodiment of the invention; and,

[0013] Figure 5 depicts an exemplary layout of several novel DRAM cells formed according to the fabrication techniques of the present invention.

Detailed Description

[0014] Figure 1 shows a cross-sectional view of the DRAM cell 10 having a storage cell 20 and a control cell 30 separated by a p-well region 45 manufactured in accordance with vertical trench DRAM technology. The storage cell 20 includes a vertical pass transistor device 25, for example, a MOSFET device, fabricated on a deep trench capacitor, for con-

trolling the receipt, storage and retrieval of voltage in the deep trench capacitor 29. Particularly, data information comprising a voltage present on a bit line (BL) is stored in the capacitor 29 when a channel formed in the p-well conducts voltage from the bitline to the connected deep trench capacitor via a buried strap 50 and diffusion region 28 when the MOSFET device is turned on. This occurs, for instance, in response to application of a wordline (WL) voltage connecting a gate 27 of the vertical storage cell MOSFET device 25 during a DRAM write or read operation. Electrical connection of the bitline BL conductor to trench capacitor 29 is enabled by the pass transistor device 25 that enables channel conductivity to the buried strap diffusion region 50 of n+ type material upon application of a WL voltage to storage cell gate 27. The control cell 30 includes a vertical MOSFET device 35 that further responds to application of the wordline (WL) voltage for controlling the voltage of the p-well structure 45 in vertical DRAM technology. That is, the storage cell 20 and control cell 30 share the same WL. The control cell 30 additionally includes a buried strap diffusion region 60 of n+ type material, however, is lower in depth than the storage cell buried strap 50. That is, the IT depth of the control cell is

below the second BS. Compared with the current IBM 110nm DRAM technology, isolation trenches (IT) depth needs to be deeper, and a more advanced IT fill process such as SOG is used to fill the IT, as will be described in greater detail hereinbelow.

[0015] In the detailed cross-sectional view of the DRAM structure 10 including storage cell MOSFET and control cell MOSFETs 20,30 shown in Figure 1, each storage and control cell 20, 30 is formed on a substrate having an n-type doped region forming a buried plate 18. The storage cell device 25 further includes a source region 26 doped with n+ type material, a P-type well 45 and a drain diffusion region 28 doped of n+ type material. The capacitor 29 is a deep trench type formed within a substrate, having an isolated region 23 filled with polysilicon material. The polysilicon conductor is isolated with a collar dielectric material 46, e.g., an oxide, separating the drain diffusion from a buried plate region of n type silicon, for example. The gate 27 of the storage transistor 25 is isolated from the conductor 23 of the deep trench capacitor 29 by a top trench dielectric layer 24, e.g., an oxide. The control cell device 35 includes the buried strap 60 of n+-type material and with a gate 37 and a gate dielectric 34. The con-

trol cell gate 37 is connected to the n+ diffusion buried strap (BS2) 60 and influences a n-type doped diffusion layer 38 formed in a later thermal process in the p-well when receiving the WL voltage. That is, as will be described, in response to application of the wordline voltage, a depletion region is formed in the p-well 45 which functions to control p-well voltage and hence improve performance of the storage cell 20.

[0016] Figures 2(a) and 2(b) illustrate more clearly the operation of the novel DRAM control cell 30 for controlling the p-well voltage with Figure 2(a) illustrating a depletion region 75 formed in the p-well 45 at the location of the control cell 20 buried strap 60 for controlling p-well voltage when the WL is at an off state (e.g., WL at 0 volts). Figure 2(b) illustrates the depletion region 76 formed at the location of the control cell 20 buried strap 60 for controlling p-well voltage when the WL is in an active state (e.g., WL at positive voltage such as 3 V 4 V, for example). Particularly, as described with respect to Figures 2(a) and 2(b), when the p-well is connected at negative voltage such as 0.5V, for example, and WL is at ground, the lower buried strap 60 and resulting p-well depletion region 75 does not pinch off the p-type well 45. That is, at off-state, the control

cell gate is at 0V, the depletion region 75 formed by the BS diffusion in the p-well does not block the path between p-well1 45a and p-well2 45b. Because of the body bias effect, a high enough Vt1 is achieved to achieve low off-state leakage current. As a result, the applied negative p-well voltage is sufficient to keep the Vt high enough to suppress the sub-threshold voltage in the storage cell MOSFET.

[0017] As shown in Figure 2(b), when the WL is at an active state, the control cell 20 buried strap 60 is at high voltage, the depletion region 76 formed between the BS 60 and p-well is sufficient to pinch off the top p-well (pass transistor p-well2) and bottom p-well (p-well1 connected to a contact). The p-well 45b will thus be at a floating state, thereby improving gate drive current. That is, when the gate is activated, the depletion regions between formed in the p-well at BS 60 extends sufficiently toward the storage cell collar dielectric 45 to render the top p-well1 45b at floating condition. Utilizing current doping profiles, the depletion width has at least a 50nm difference with WL at 3.0 volts versus 0.0 volts. Therefore, at this condition, the threshold voltage Vt2 is smaller than Vt1 and may range from 200 mV to 500 mV. Thus, the storage cell transistor

can have more gate over drive and drive current.

[0018] It should be understood that in an alternative embodiment, shown in Figure 3(a) and 3(b), a (2- sided or 4-sided) vertical transistor device 90 comprising two trenches is provided. According to the invention, the device includes respective two first buried straps (BS1) functioning as a drain (or source) diffusion region for the device and two second buried straps (BS2) functioning to provide control diffusions are formed in the p- well region. In each trench of the transistor device shown, the two first buried straps (BS1) are at an equal trench depth and the two second buried straps (BS2) and control diffusions 71, 72 are at an equal trench depth below the corresponding first buried straps formed in the p- well. In this embodiment, the threshold voltage of the vertical transistor device is controlled in accordance with depletion regions formed by application of a voltage at the device gate, at both second buried strap regions and corresponding diffusions, that extend sufficiently into the p-well and merge to effectively pinch off the p- well region to disconnect the p-well region into two regions, a first conductive and second floating p-well region, wherein the floating p-well region enables a lower threshold voltage

for turning on the vertical transistor device.

[0019] Thus, upon condition of off-state, the gate is at 0V, the depletion regions 73, 74 of respective BS2 diffusions 71, 72 in the p-well does not block the path between p-well1 45a and p-well2 45b. Because of the body bias effect, a high enough Vt1 is achieved to achieve low off-state leakage current. Upon condition of active-state, WL active (voltage > 0, e.g., 3V- 4V), the depletion regions 73", 74" of respective BS2 diffusions 71, 72 in the p-well at BS 50" and 60" extend sufficiently toward each other and merge together such that the top p-well1 45b is at floating condition. Therefore, at this condition, the threshold voltage Vt2 is smaller than Vt1, the storage cell transistor can have more gate over drive and drive current.

[0020] A method for manufacturing the DRAM cell of the invention including two trenches, one trench for storing the data and the second trench for controlling the p-well voltage, which, in effect, places part of the p-well in a floating condition thus decreasing the threshold voltage as compared to when the transistor is in an off-state is now described with respect to Figures 4(a)-4(o).

[0021] As shown at step 100 in the Process Flow diagram for fabricating the DRAM cell of Figure 4 (a), implementing

deep trench lithography and patterning, deep trenches 200, 300 are formed in a doped P-type Si substrate using an etching technique such as Reactive ion etch (RIE). The trenches may range from between 5.0 and 8.0 micrometers deep, for example. Patterning includes use of a nitride or like materials, as the hard mask 198 for Si etch and, as shown, two deep trenches 200, 300 forming the DRAM Cell 10 of the invention result. The first deep trench 200 forms the data storage cell 20 and the second deep trench 300 for forming the control cell 30 to control the p-well voltage and improve DRAM cell gate drive and reduce leakage. After trench formation, a dielectric layer 210, 310 for the trench capacitor is formed on the sidewalls of each deep trench. The dielectric can be oxide, or an oxynitride, or other materials such as a high-K material in order to improve gate capacitance. As shown at step 103 of the Process Flow depicted in Figure 4(b), each deep etch 200, 300 is filled with an n+ doped Polysilicon 205, 305 by a chemical vapor deposition (CVD) or like deposition process. To fill each deep trench, multiple deposition and etch processes have to be used. The resulting structure after polysilicon fill is shown in Figure 4 (b). As shown at step 106 of the Process Flow depicted in Figure

4 (c), each filled deep trench 200, 300 is recessed by a RIE process to a common depth. In the next step 110 depicted in Figure 4 (d), a dielectric material, such as an oxide, is deposited, by a CVD process, in each trench 200, 300. The dielectric layer 215, 315 formed is thinner on the side-wall than it is on the polysilicon fill 205, 305. The resulting structure is shown in Figure 4 (d). Then, in the next step 113 depicted in Figure 4(e), the oxide 215, 315 previously deposited on each side wall is etched away by an etchant such as diluted HF, for example, or like etchant types. The oxide 215 above polysilicon 205 in the storage cell is completely etched away while the oxide 315 in the control cell partially remains as shown in the resulting structure of Figure 4(e). This is enabled by implementing lithography and patterning while the storage cell is covered by photoresist during the oxide etch.

[0022] Further, in the next step 117, a dielectric layer such as an oxide layer 220, 320 is deposited in the trenches 200, 300 to a thickness ranging between 20nm - 30nm, by a deposition process such as CVD. The oxide above the polysilicon in the storage cell is further etched away by RIE and the resulting structure is depicted in Figure 4(f). Then, in the next step 120, another n+-type doped polysilicon

layer 225, 325 is deposited in the trenches 200, 300 by a CVD process. Then in each trench, the polysilicon is etched back, e.g., recessed to a depth ranging from between about 300 nm to 500 nm, by an etching process such as RIE. The resulting structure is shown in Figure 4(g). The recess depth for the storage cell determines the channel length of the vertical pass transistor. In a further step 123, the storage cell is covered by a photoresist material and the polysilicon 325 in the control cell trench 300 is recessed to a depth ranging from between about 400 nm 700 nm, for example, as shown in Figure 4(h). This determines the location of the control cell buried strap 60. In a further step 127, the oxide layer 220, 320 on the side-walls of each trench 200, 300 deposited at step 117 (Figure 4(f)), is etched away by a wet etch process. A very thin nitride layer is deposited on the side-wall to protect the side-wall (diffusion barrier). Polysilicon (e.g., n+-type doped) material 230, 330 is then deposited in each trench 200, 300 and recessed by a RIE process with the resulting structure shown in Figure 4(i). This n+ - type doped polysilicon 230, 330 is deposited to form the storage cell and control cell buried straps 50, 60 and n+ diffusion regions which, in the storage cell, connects the

pass transistor to the capacitor in the device 10 of Figure 1. The n -type dopant in the buried straps diffuses into the silicon to form the n-type diffusion regions 28, 38 in the device 10 of Figure 1. In a next step 130, as was described herein with respect to Figures 4(d) and 4(f), dielectric material such as an oxide 235 is first deposited and etched away on the side-walls of each deep trench 200, 300 and completely removed from the control cell with the resulting structure shown in Figure 4(j). The oxide remaining in the storage cell comprises the top trench dielectric layer 24 in the device 10 of Figure 1. In a next step 133, a nitride layer 240 is then deposited in each trench 200, 300 and, in a subsequent process step, is completely etched away in the control cell trench 300 as shown in Figure 4(k).

[0023] In a further step 137, a dielectric layer 245, 345 ranging between 10nm - 20nm in thickness is deposited by a deposition process such as chemical vapor deposition in each trench 200, 300. Dielectric materials include an oxide, oxynitride or other like dielectric materials. Further, the dielectric layer is etched by an RIE process and the resulting structure is shown in Figure 4(l). At next step 140, polysilicon 250, 350 is then deposited (CVD or like depo-

sition process) in each of the remaining trenches 200 and 300 and planarized by a polished by chemical mechanical polishing (CMP) process. The resulting structure is shown in Figure 4(m). In a further processing step 143, the polysilicon, oxide and nitride layers in the storage cell 20 are etched away by a wet chemical process. Given the variety of the layers, different etching process may be employed for removing each layer, one layer at a time. The control cell is covered by a photo resist during the wet etch process. The resulting structure is shown in Figure 4(n). A gate dielectric layer 255 is then formed in the storage cell in the next process step 147. This layer can be materials such as oxide, nitride, or high-k material. The process can be thermal, CVD depending on the material used. The resulting structure is depicted in Figure 4(o). The dielectric layer 255 forms the gate oxide of the vertical pass transistor device 10 of Figure 1. Preferred gate dielectric materials include an oxide, oxynitride, and the like. In a final processing step 150, polysilicon 260 (e.g., n+ type doped) forming the gate conductor is deposited in each cell by a CVD process and planarized/polished by CMP process. The resulting structure is shown in Figure 4(p).

[0024] The remaining process steps include the same processing steps required to form the DRAM by implementing conventional DRAM processes, for example, including interconnect wiring to form the DRAM cell.

[0025] Figure 5 depicts an exemplary layout 80 of several novel DRAM cells 10a, 10b, . . . 10f, formed according to the fabrication techniques of the present invention. The size for each cell is 8F2 which is the same as current 110 nm DRAM technology. Each DRAM cell 10a, 10b, 10c includes the respective vertical pass transistor storage cells 20a, 20b, 20c and control cells 30a, 30b, 30c all connected to wordlines WLa, WLb, WLc. Each DRAM cell 10d, 10e, 10f includes the respective vertical pass transistor storage cells 20a, 20b, 20c and control cells 30a, 30b, 30c all connected to wordlines WLa, WLb, WLc. Each DRAM cell 10d, 10e, 10f includes the respective vertical pass transistor storage cells 20d, 20e, 20f and control cells 30a, 30b, 30c all connected to wordlines WLa, WLb, WLc. Thus, in the layout depicted in Figure 5, each control cell 30a, 30b, 30c is fabricated to effect the floating p-well condition for two adjacent vertical pass transistors (deep trench storage cells). Additionally shown in Figure 5 are two bitlines BL1, BL2, with BL1 shown connecting source regions

(not shown) of vertical pass transistors storage cells 20a, 20b, 20c and BL2 shown connecting source regions (not shown) of vertical pass transistors storage cells 20d, 20e, 20f.

[0026] While there has been shown and described what is considered to be preferred embodiments of the invention, it will, of course, be understood that various modifications and changes in form or detail could readily be made without departing from the spirit of the invention. It is therefore intended that the invention be not limited to the exact forms described and illustrated, but should be constructed to cover all modifications that may fall within the scope of the appended claims.